Notice of Allowability	Application No.	Applicant(s)
	10/059,392	TAUCHI ET AL.
	Examiner	Art Unit
	Thomas H Parsons	1745

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed 18 February 2004*.

2. ☒ The allowed claim(s) is/are *1-4*.

3. ☒ The drawings filed on *18 February 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/~~Comment~~
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney Robert Pous on 13 April 2004.

The application has been amended as follows:

Page 11, Abstract, line 1, each occurrence of "a" has been deleted; and,

line 2, each occurrence of "a" has been deleted.

2. The following is an examiner's statement of reasons for allowance:

U.S. Patent No. 5,429,680, issued to Fuschetti on 4 July 1995 discloses a first soldering layer formed of a first soldering agent (i.e. a low temperature solder) at a position to connect a heat-radiation side insulating substrate and a case); and a second soldering layer formed of a second soldering agent (i.e. a low temperature solder) at a position to connect a heat-radiation side insulating substrate and one end of each of a plural P-type and N-type semiconductor chips, the second soldering layer also connecting a heat-absorption side insulating substrate and the other end of each of the plural P-type and N-type semiconductor chips.

Fuschetti does not teach or suggest the second soldering agent being identical with the first soldering agent in raw material.

Fuschetti also discloses in another embodiment a first soldering layer formed of a first soldering agent (i.e. a low temperature solder) at a position to connect a heat-radiation side insulating substrate and a case); and a second soldering layer formed of a second soldering agent (i.e. a high temperature solder) at a position to connect a heat-radiation side insulating substrate and one end of each of a plural P-type and N-type semiconductor chips, the second soldering layer also connecting a heat-absorption side insulating substrate and the other end of each of the plural P-type and N-type semiconductor chips.

Fuschetti discloses the raw material for the second or high temperature solder but fails to teach or disclose the second soldering agent being identical with the first soldering agent in raw material.

In yet another embodiment, Fuschetti discloses a first soldering layer formed of a first soldering agent (i.e. a high temperature solder) at a position to connect a heat-absorbing side insulating substrate and a heat sink, and a second soldering layer formed of a second soldering agent (i.e. a high temperature solder) at a position to connect a heat-radiation side insulating substrate and one end of each of a plural P-type and N-type semiconductor chips, the second soldering layer also connecting a heat-absorption side insulating substrate and the other end of each of the plural P-type and N-type semiconductor chips.

However, Fuschetti fails to teach or suggest the second soldering agent being identical with the first soldering agent in raw material with the first soldering agent being at a position to connect a heat-radiation side insulating substrate and a case.

In contrast, the instant invention comprises a second soldering agent being identical with the first soldering agent in raw material with a first soldering layer formed of a first soldering agent at a position to connect a heat-radiation side insulating substrate and a case, and a second soldering layer formed of a second soldering agent at a position to connect a heat-radiation side insulating substrate and one end of each of a plural P-type and N-type semiconductor chips, the second soldering layer also connecting a heat-absorption side insulating substrate and the other end of each of the plural P-type and N-type semiconductor chips.

The instant specification discloses that using a first and second solder identical in raw material is critical to providing a thermoelectric module having improving connection reliability and heat resistance, and free from thermal deformation or leakage.

For this reason, claim 1 and claim 3, which is dependent thereon, and claim 2 and claim 4, which is dependent thereon are patentably distinct from the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas H Parsons whose telephone number is (571) 272-1290. The examiner can normally be reached on M-F (7:00-4:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pat Ryan can be reached on (571) 272-1292. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas H Parsons
Examiner
Art Unit 1745

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Patrick Ryan
Supervisory Patent Examiner
Technology Center 1700